Remarks

Examiner Berezny is thanked for the thorough Office Action.

Election/Restriction

Applicant acknowledges the final of the requirement of with respect to the applicant's traverse of the invention's claims 1-8.

Please cancel non-elected claims 9-14. These claims will be prosecuted in a division patent application at a later date.

In the Specification

The specification has been reviewed and amendments made to correct typographical and editorial errors. No new matter has been added.

The objections to the Specification

A. Page 10, lines 4- 6 are amended. "bit line region" is changed to –node cell region.--

B. Page 12, lines 9 -19 are amended. The text [lightly doped] is deleted.

CLAIM REJECTIONS:

Rejection of claim 7 under 35 U.S.C. §112

The Office Action dated 7/18/2002 in paragraph 4 rejects claim 7. The specification on p. 9, lines 11 to 18 teaches that two separate masking and implant steps can be used to form the bit line region and cell node regions with different dopant concentrations. For this reason, claim 7 is believed to be allowable.

Rejection of claims 1- 7 under 35 U.S.C. §112 2nd paragraph

The Office Action dated 7/18/2002 in paragraph 6 rejects claims 1-7.

Claim 1, step b is amended to delete the extraneous text "said cell node region". This is a typographical error.

Rejection of claim 7 under 35 U.S.C. §112 2nd paragraph

The Office Action dated 7/18/2002 in paragraph 7 rejects claim 7. The specification on p. 9, lines 11 to 18 teaches that two separate masking and implant steps can be used to form the bit line region and cell node regions with different dopant concentrations. Claim 1, step b does not limit the implantation of ions to one implant step. Furthermore the spec discloses that the implantation can be in two steps. See spec. on p. 9, lines 11 to 18. For this reason, claim 7 is believed to be allowable.

The Rejection Of Claim 1 Under 35 U.S.C. § 103(a) In View Of Gilgen et al.

The rejection of claim 1 under 35 U.S.C. § 103(a) in view of Gilgen et al. is acknowledged.

Claim 1 is non-obvious over Gilgen et al.

Claim 1 is non-obvious over Gilgen et al. because Gilgen et al. uses different steps to form a different structure than claim 1. The table below shows some of the differences between the process of claim 1 and Gilgen et al.

Table: Differences between claim 1 and Gilgen et al.

Claim 1	Gilgen et al.
1. A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:	
a) FIG 1 forming a word line structure 18 24 and a capacitor plate structure 20 30 on a substrate 10;	**Different** – See below. capacitor plate structure 151 161 is over a gate 101 and FOX 71, not on the substrate 11. See fig 16
(1) a capacitor plate structure 20 30 comprised of a capacitor dielectric 20 **on** said substrate 10 and a conductive plate layer 30 on said capacitor dielectric 20; said capacitor plate structure 20 30 overlying a plate region of said substrate; said plate region and said conductive plate layer 30 acting as plates of a capacitor;	**Different** – The capacitor dielectric layer 152 is not no the substrate 11 See fig 16. **Different** – Gilgen's Capacitor bottom plate 151 is a poly layer . In contract, claim 1's capacitor bottom plate is a "plate region" of the substrate.
(b) FIG 2 implanting ions of a first conductivity type into said substrate forming a cell node region 40 in said substrate 10 between said word line structure 18 24 and	

said capacitor plate structure 20 30; and forming a first bit line region 34 in said substrate adjacent to said word line structure 18 24, said cell node region 40 and said first bit line region 34 do not intersect;	
(c) forming spacers 46 50on the sidewalls of said word line structure 18 24 and said capacitor plate structure 20 30;	**Different** – Spacers 171 161 Fig 17 – spacers 171 are not formed on the capacitor plates 151 161. Also 161 is not a spacer but a cap plate.
d) FIG 3 forming a mask pattern 56 over said cell node 40;	
e) implanting ions of a first conductivity type into said substrate to form a second (high concentration) bitline region 60; and not implanting ions into said cell node;	
f) FIG 4 removing the mask pattern 56;	
g) FIG 4 forming a dielectric layer 52 over said substrate; and	
h) FIG 4 forming a bitline contact 68 to said second (high concentration) bitline 60 region.	

- Note the element numbers and fig #'s in the table above do not limit the interpretation of the claim or other claims.

As shown above in the figs, Gilgen does not form the applicant's claimed 1T SRAM device.

Claim 1, step a, is non-obvious because Gilgen's capacitor plate structure 151 161 is over a gate 101 and FOX 71, not on the substrate 11. See fig 16

Claim 1, step a) (1) is non-obvious because **Gilgen's** capacitor dielectric layer 152 is not no the substrate 11 See fig 16. Also, Gilgen's Capacitor bottom plate 151 is a poly layer . In contract, claim 1's capacitor bottom plate is a "plate region" of the substrate.

Claim 1, step c is non-obvious because Gilgen's Spacers 171 161 Fig 17 – spacers 171 are not formed on the capacitor plates 151 161. Also 161 is not a spacer but a cap plate.

There are addition non-obvious differences seen in Gilgen's figs. Most importantly, Gilgen does not form applicant's 1T SRAM.

Rejection of claims 2, 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen as applied to claim 1 and further in view of Mandelman

The rejection of claims 2, 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen as applied to claim 1 and further in view of Mandelman is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the following comments.

Applicant could not find the cited information form Mandelman as stated in the Office Action paragraph 10. For example, there is no claim 18.

First, it is not obvious to combine the references. Neither reference suggest they be combined, nor do they solve related problem. Importantly, neither reference forms applicant's 1T-SRAM cell.

Mandelman forms a different device, a n-type MOSFET for a DRAM, Not applicant's 1T-SRAM cell. See Mandelman claim 1 preamble, background of invention.

Mandelman forms N doped regions in contrast to applicant's N-type node and bitline. The Office Action para 10 posits that it known in the art to switch N and P type devices. However, while n and p devices are know, it is not known to switch p and n dopants because N and P dopants and type device have different electrical properties. This is especially true with doping concentration. Therefore, is it not obvious to switch doping types. This switch could only be done by hindsight.

Moreover, Mandelman does not for the same 1T-SRAM device as the applicant and it is not obvious to apply the teaches of Mandelman to the applicant's invention. For example, Mandelman performs a N+ implant into the bitline to lower the resistance of W studs. See col. 3, 60-64. There is no motivation to do this implant in the applicant's device. Moreover, Mandelman does not suggest the advantage of an implant in applicants' 1T SRAM cell.

Rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi

The rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

First, it is not obvious to combine the references. Neither reference suggest they be combined, nor do they solve related problem. Importantly, neither reference forms applicant's 1T-SRAM cell.

Second, it is further non-obvious to apply Chi to the invention and the other references because Chi does not even form the applicant's p-type device. The Office Action para 5 admits that Chi forms the wrong (n-type) devices. For the reasons stated above, it is not obvious to switch n to p, especially in wells concentrations.

Rejection of claims 8 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi and further in view of Wolf, vol. 2, p. 589

The rejection of claims 8 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi and further in view of Wolf, vol. 2, p. 589 is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the comments.

Claim 8 contains the limitation of non-obvious claims 1 to 7. Claim 8 is non-obvious for the reasons discussed above.

New parent claim 15 is non-obvious

New parent claim 15 is non-obvious because claim 15 contains the limitations of non-obvious claim 1 and additional limitations.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectfully requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone the undersigned attorney George Saile at (845) 452-5863 should there be anyway that we could help to place this Application in condition for Allowance.

Respectfully submitted,

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Appendix

Version with markings to show changes

In the specification

The 1st full Paragraph on spec p. 10 has been amended as follows:

In a critical step in the invention, as shown in FIG 3, we form a mask (e.g., resist) pattern 56 over the cell node 40. Any implant blocking mask can be used. This resist pattern servers to block a subsequent high concentration (e.g., P+) implant into the [bit line] node cell region.

The 2nd full Paragraph on spec p. 12 has been amended as follows:

The bit line region 34 60 consists of a first bit line region 34 and a second bit line [(lightly doped)] region 60. The first bit line region 34 has about the same impurity concentration as the cell node 40.

In the Claims

1.(AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM),

comprising the steps of:

a) forming a word line structure and a capacitor plate structure on a substrate;

(1) [a] said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, [said cell node region];

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;

f) removing the mask pattern;

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region.

8. (AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of :

a) forming a dielectric layer on a substrate;
forming a conductive layer on said dielectric layer;
patterning said conductive layer and said dielectric layer to form [forming] a word line structure and a capacitor plate structure on a substrate;

(1) [a] said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

(2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc;

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node regionand said first bit line region do not intersect;

(1) said first bit line region andsaid cell node region have a p-type doping and have an impurity concentration between 1E18 and 1E 19 atoms/cc,

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node; said second bitline region has a concentration between 1E20 and 1E21 atom/cc;

f) removing the mask pattern;

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region.

Please cancel claims 9 to 14

Please add new claims as shown below:

15. A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

a) forming a dielectric layer on a substrate;

b) forming a conductive layer on said dielectric layer;

c) patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;

d) forming a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

e) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region;

f) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

g) forming a mask pattern over said cell node;

h) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;

i) removing the mask pattern;

j) forming a dielectric layer over said substrate; and

k) forming a bitline contact to said second bitline region.